FIG.1

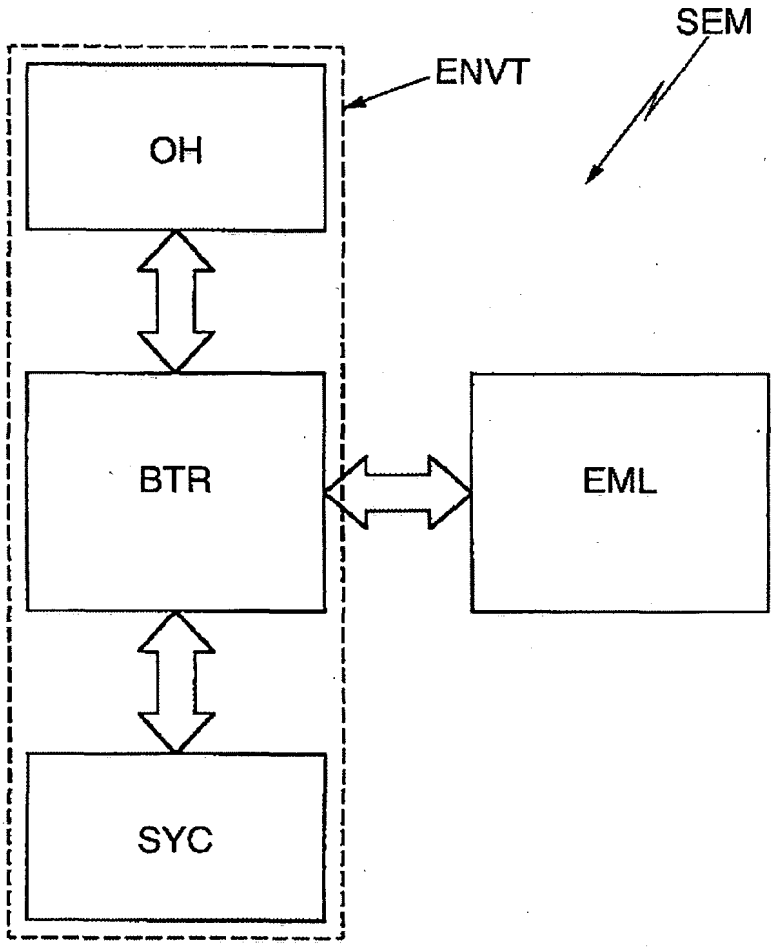

FIG.2

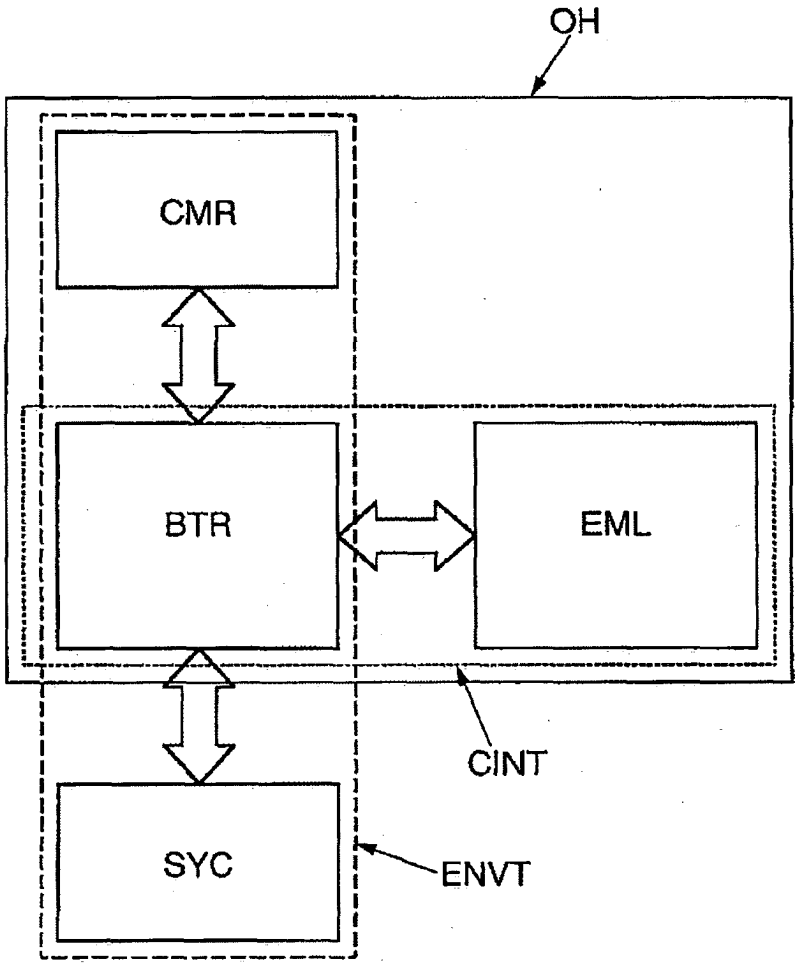

FIG.3

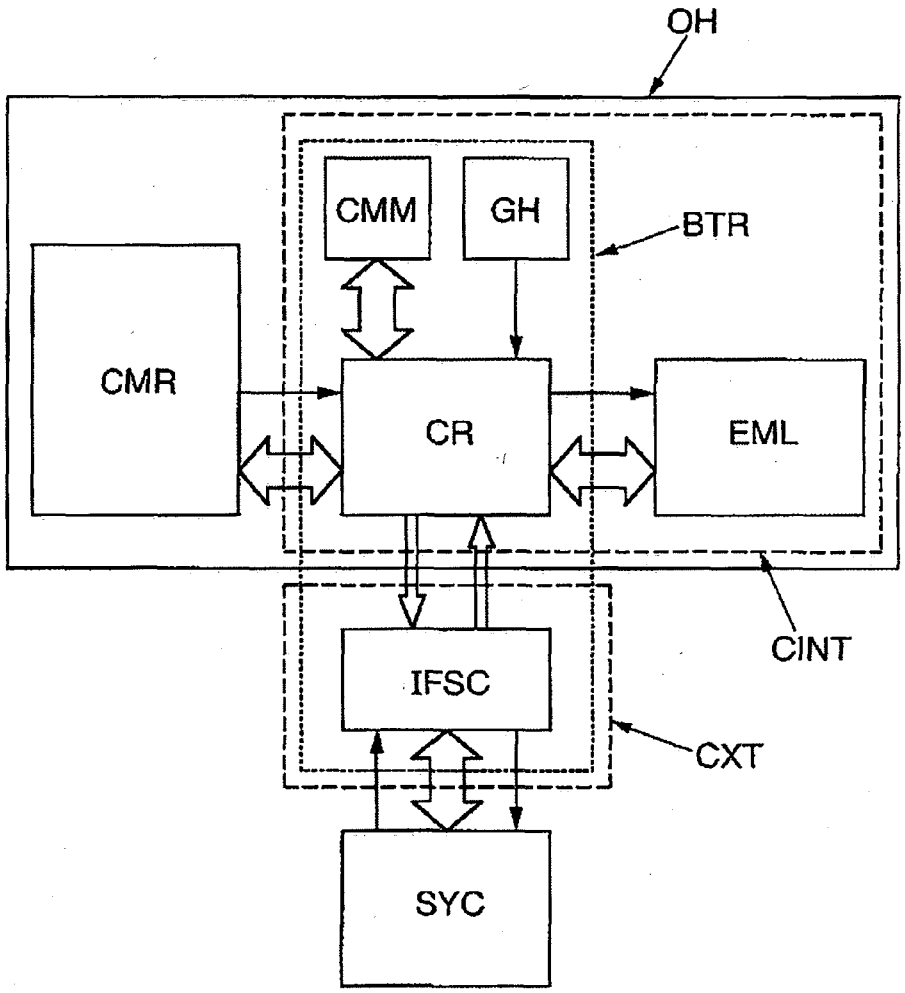

FIG.4

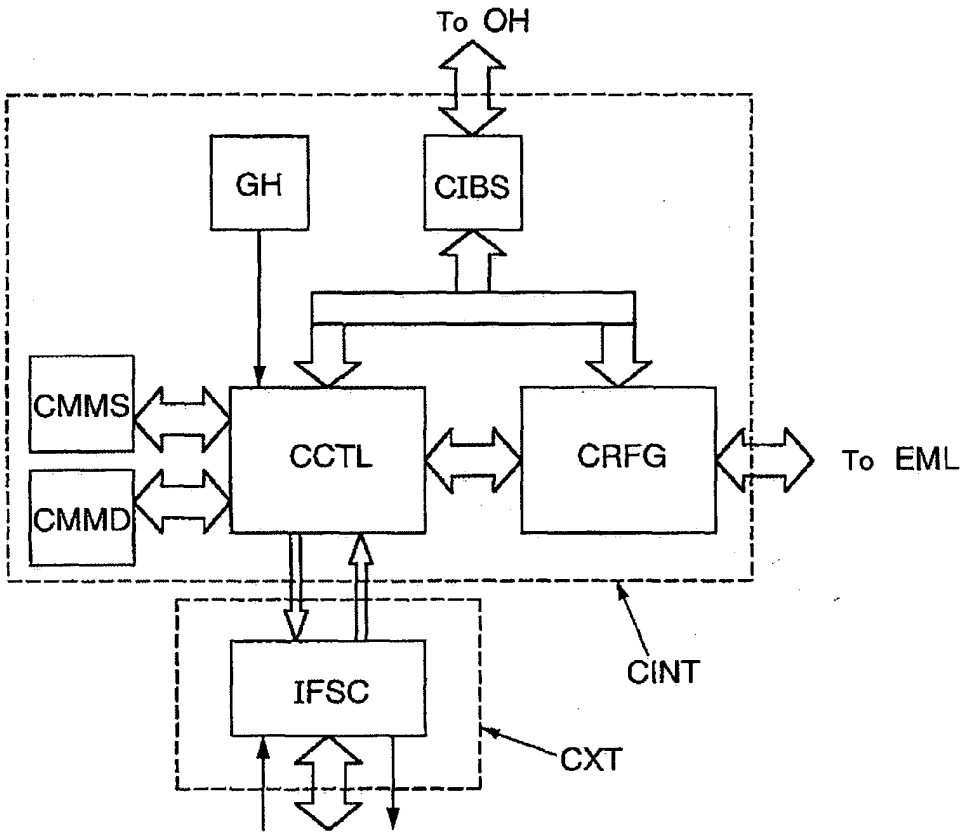

FIG.5

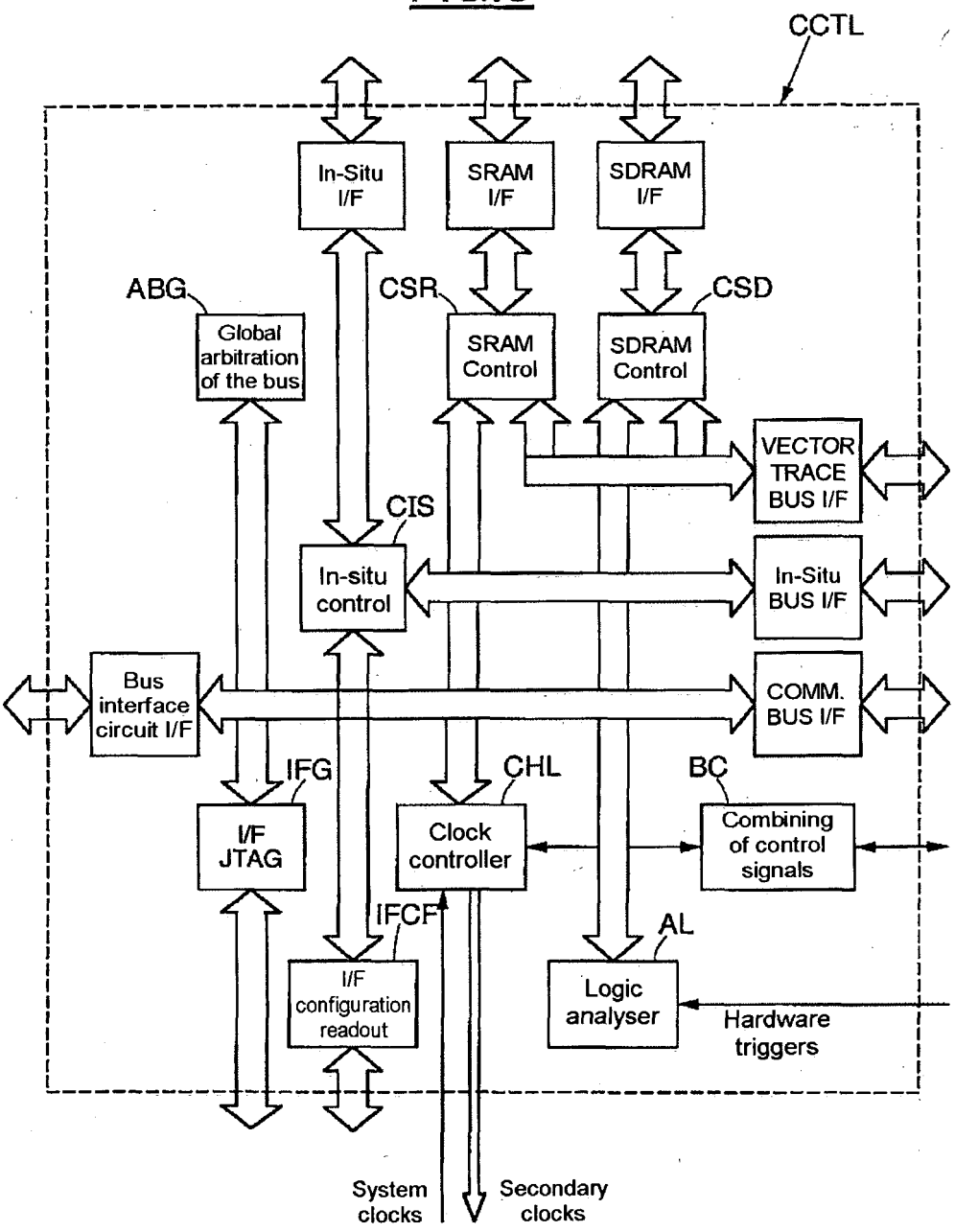
CCTL
In-Situ I/F
SRAM I/F
SDRAM I/F
ABG
CSR
CSD
Global arbitration of the bus
SRAM Control
SDRAM Control
VECTOR TRACE BUS I/F
CIS
In-situ control
In-Situ BUS I/F
Bus interface circuit I/F
COMM. BUS I/F
IFG
CHL
BC
I/F JTAG
Clock controller
Combining of control signals
IFCF
AL
I/F configuration readout
Logic analyser
Hardware triggers
System clocks
Secondary clocks

FIG.6

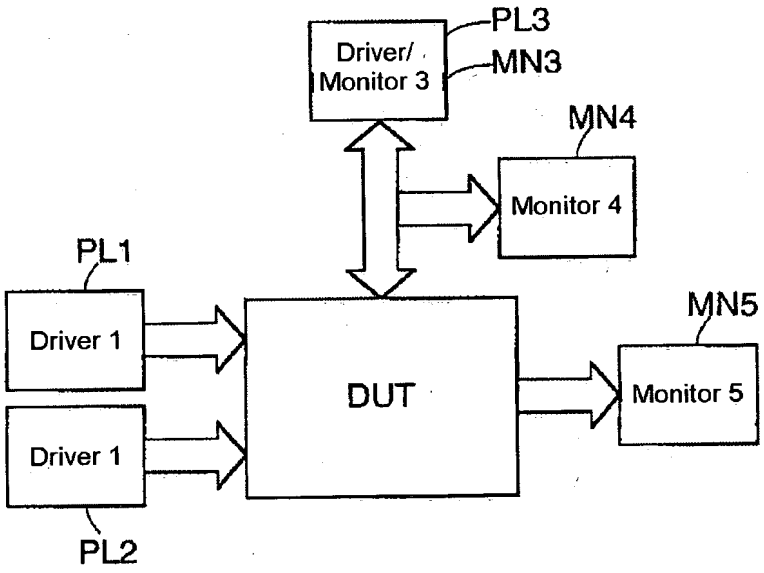
Driver/
Monitor 3
PL3
MN3
MN4
Monitor 4
PL1
Driver 1
DUT
MN5
Monitor 5
Driver 1
PL2

FIG.7a

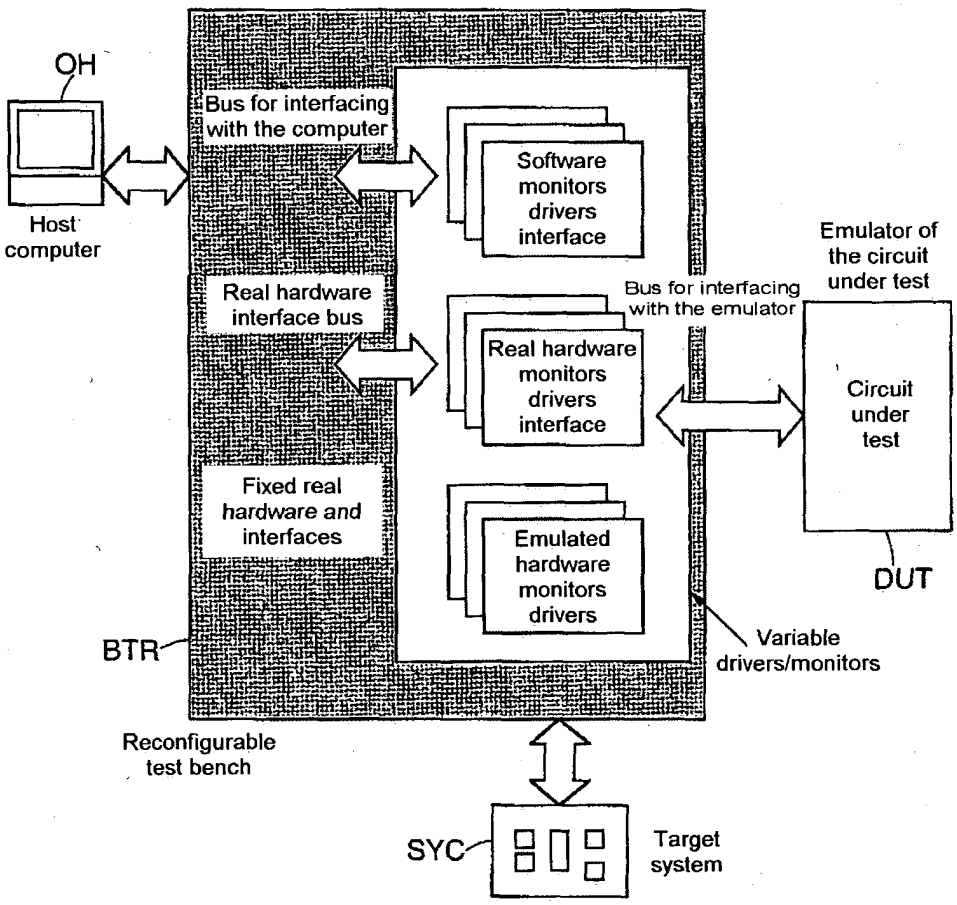
OH
Host computer
Bus for interfacing with the computer
Software monitors drivers interface
Real hardware interface bus
Real hardware monitors drivers interface
Fixed real hardware and interfaces
Emulated hardware monitors drivers
Bus for interfacing with the emulator
Emulator of the circuit under test
Circuit under test
DUT
BTR
Variable drivers/monitors
Reconfigurable test bench
SYC
Target system

FIG.7b

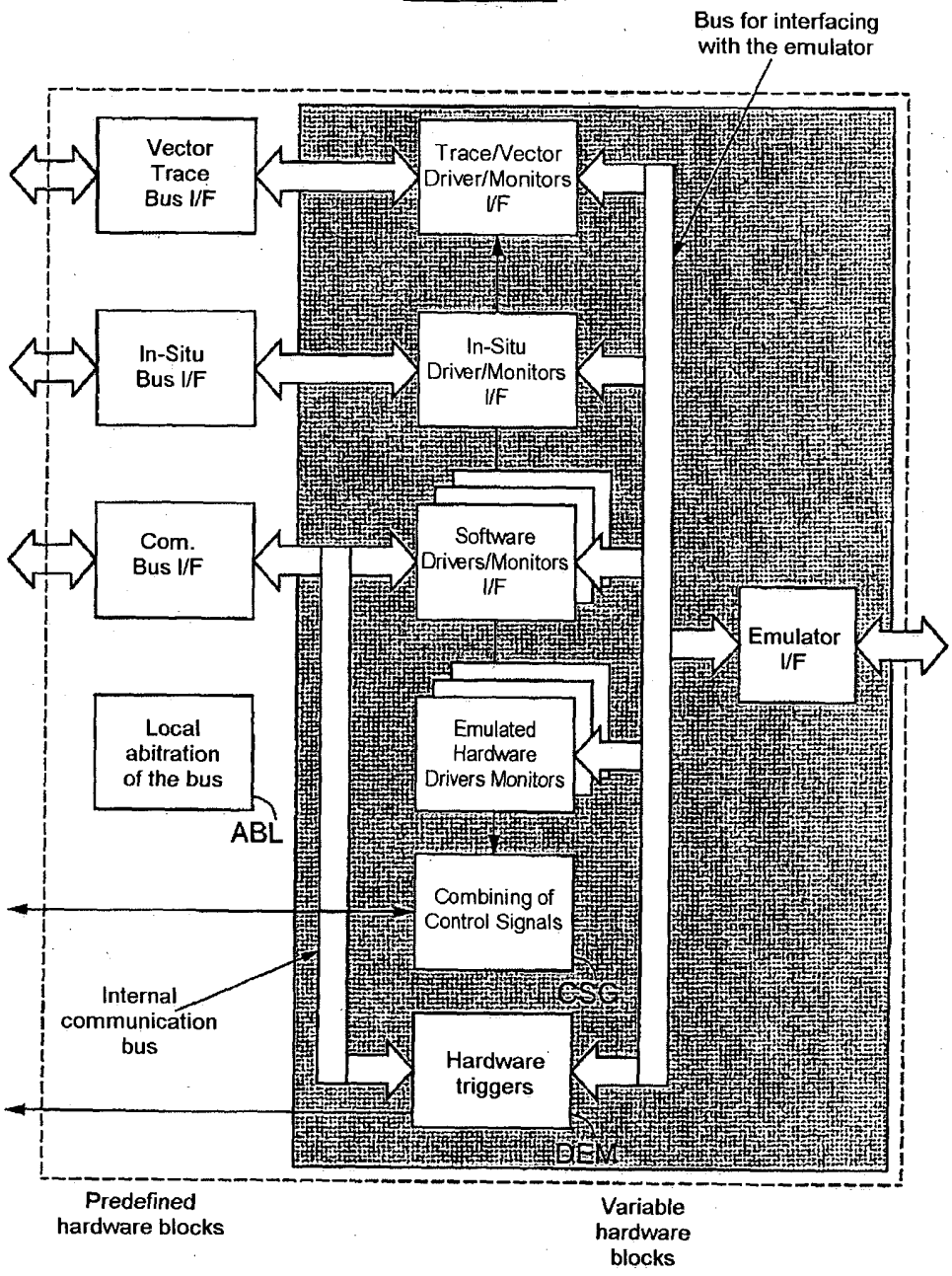
Bus for interfacing with the emulator
Vector Trace Bus I/F
In-Situ Bus I/F
Com. Bus I/F
Local abitration of the bus
ABL
Trace/Vector Driver/Monitors I/F
In-Situ Driver/Monitors I/F
Software Drivers/Monitors I/F
Emulated Hardware Drivers Monitors
Combining of Control Signals
CSG
Hardware triggers
BEM
Emulator I/F
Internal communication bus
Predefined hardware blocks
Variable hardware blocks

FIG.8

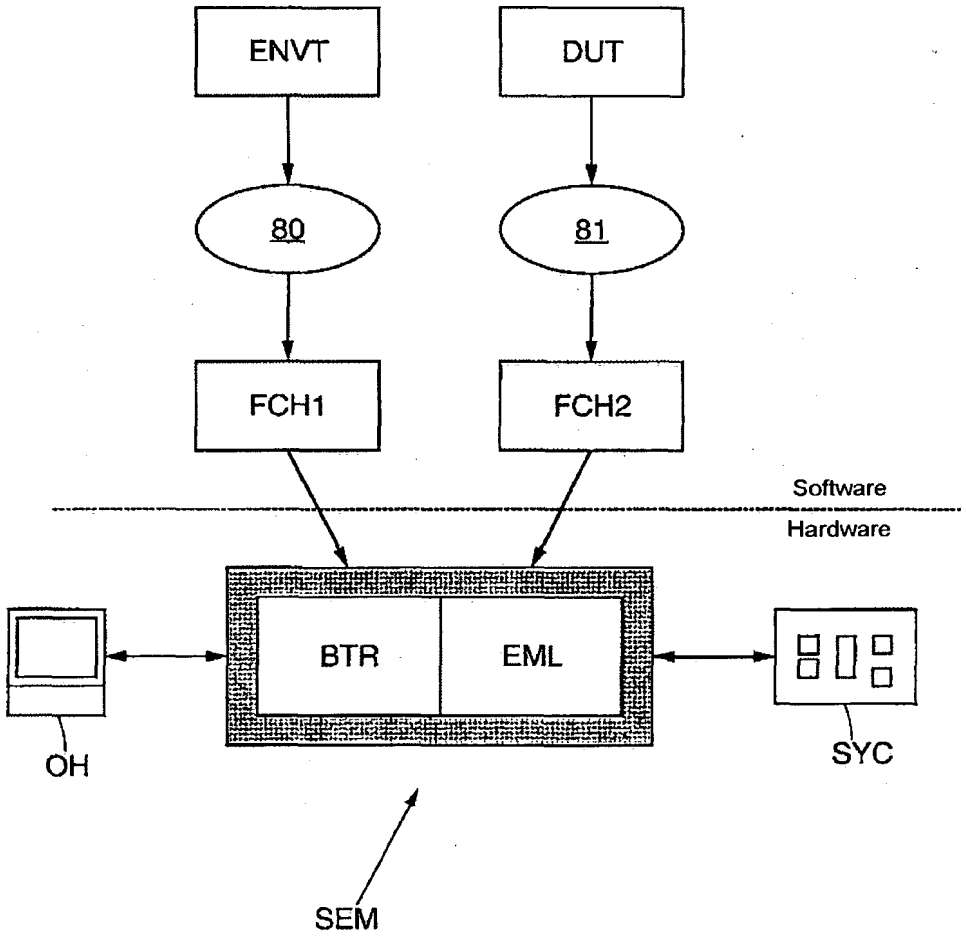

FIG.9a

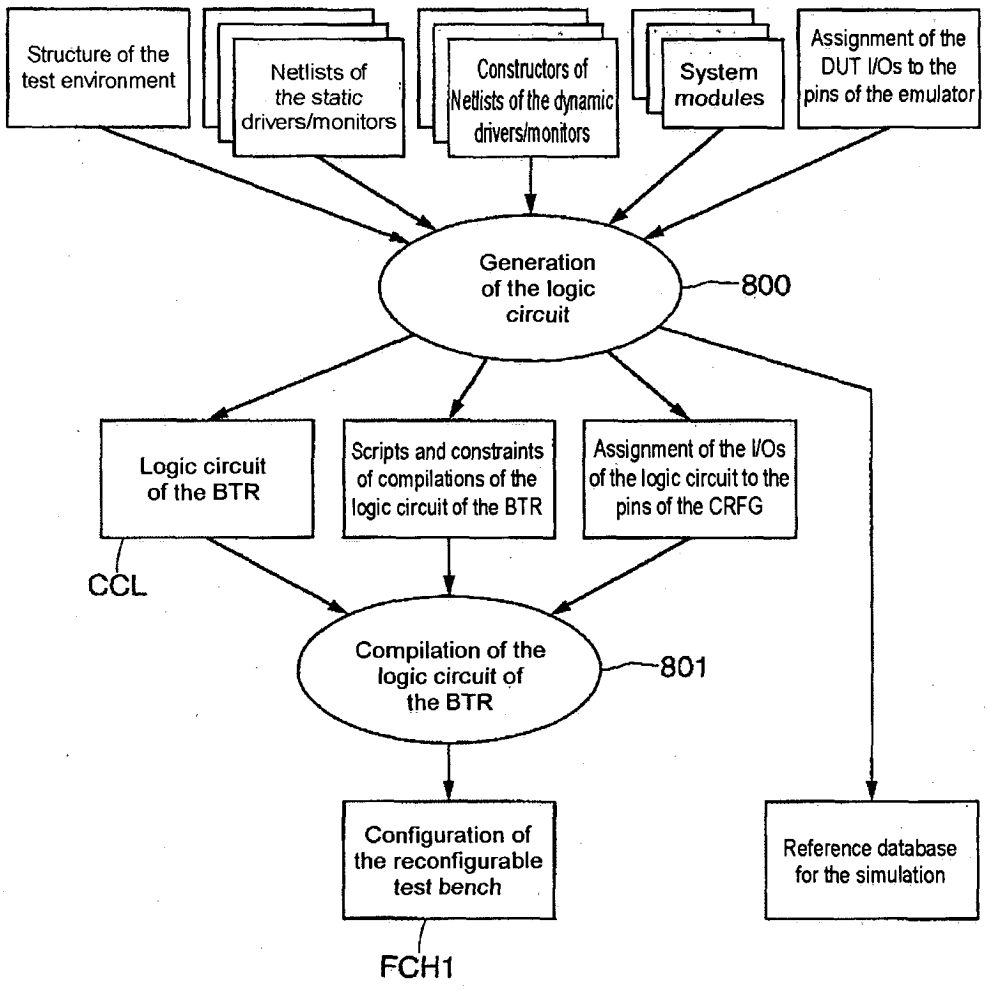
Structure of the test environment
Netlists of the static drivers/monitors
Constructors of Netlists of the dynamic drivers/monitors
System modules
Assignment of the DUT I/Os to the pins of the emulator
Generation of the logic circuit
800
Logic circuit of the BTR
Scripts and constraints of compilations of the logic circuit of the BTR
Assignment of the I/Os of the logic circuit to the pins of the CRFG
CCL
Compilation of the logic circuit of the BTR
801
Configuration of the reconfigurable test bench
Reference database for the simulation
FCH1

FIG.9b

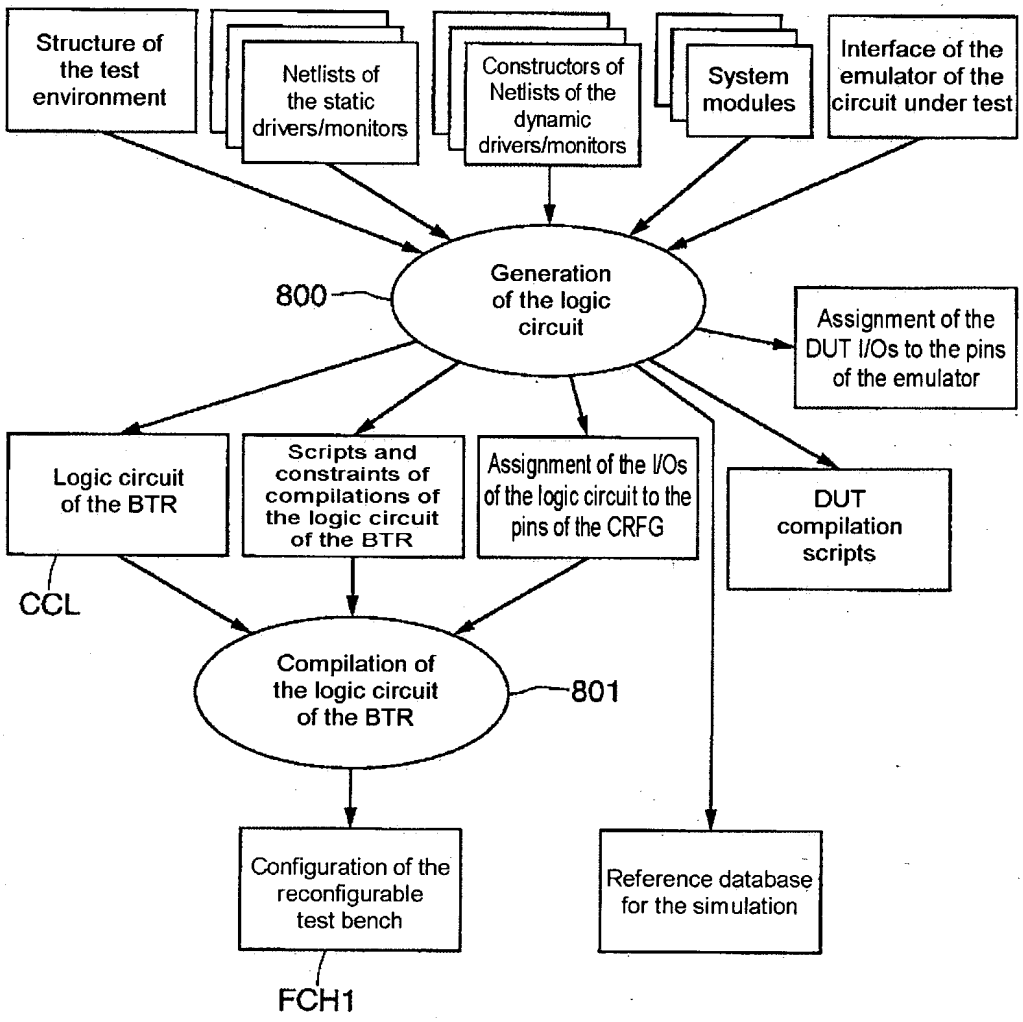
Structure of the test environment
Netlists of the static drivers/monitors
Constructors of Netlists of the dynamic drivers/monitors
System modules
Interface of the emulator of the circuit under test
800
Generation of the logic circuit
Assignment of the DUT I/Os to the pins of the emulator
Logic circuit of the BTR
Scripts and constraints of compilations of the logic circuit of the BTR
Assignment of the I/Os of the logic circuit to the pins of the CRFG
DUT compilation scripts
CCL
Compilation of the logic circuit of the BTR
801
Configuration of the reconfigurable test bench
Reference database for the simulation
FCH1

FIG.10

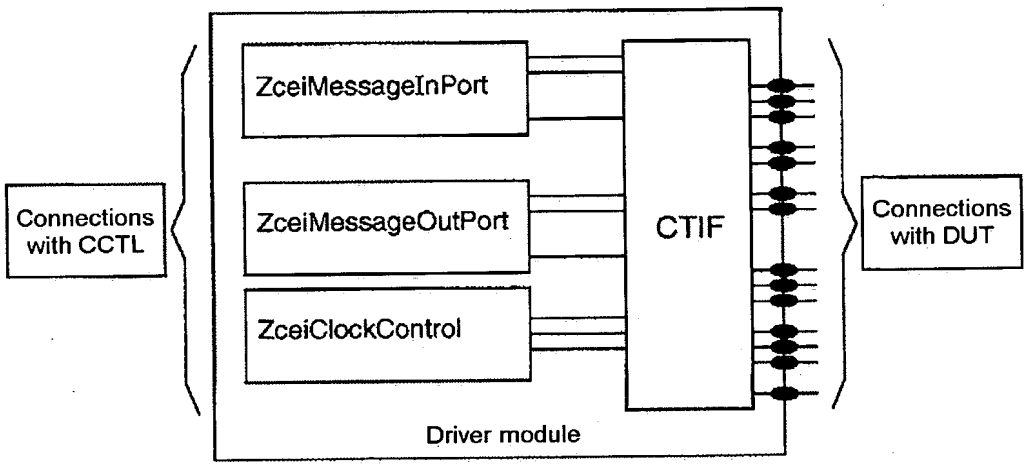
ZceiMessageInPort
ZceiMessageOutPort
ZceiClockControl
CTIF
Connections with CCTL
Connections with DUT
Driver module

FIG.11

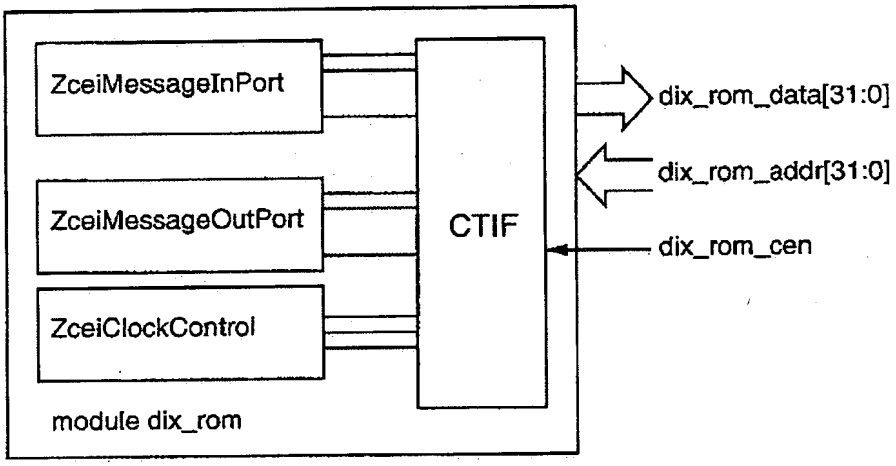
ZceiMessageInPort
ZceiMessageOutPort
ZceiClockControl
CTIF
dix_rom_data[31:0]
dix_rom_addr[31:0]
dix_rom_cen
module dix_rom

FIG.12a

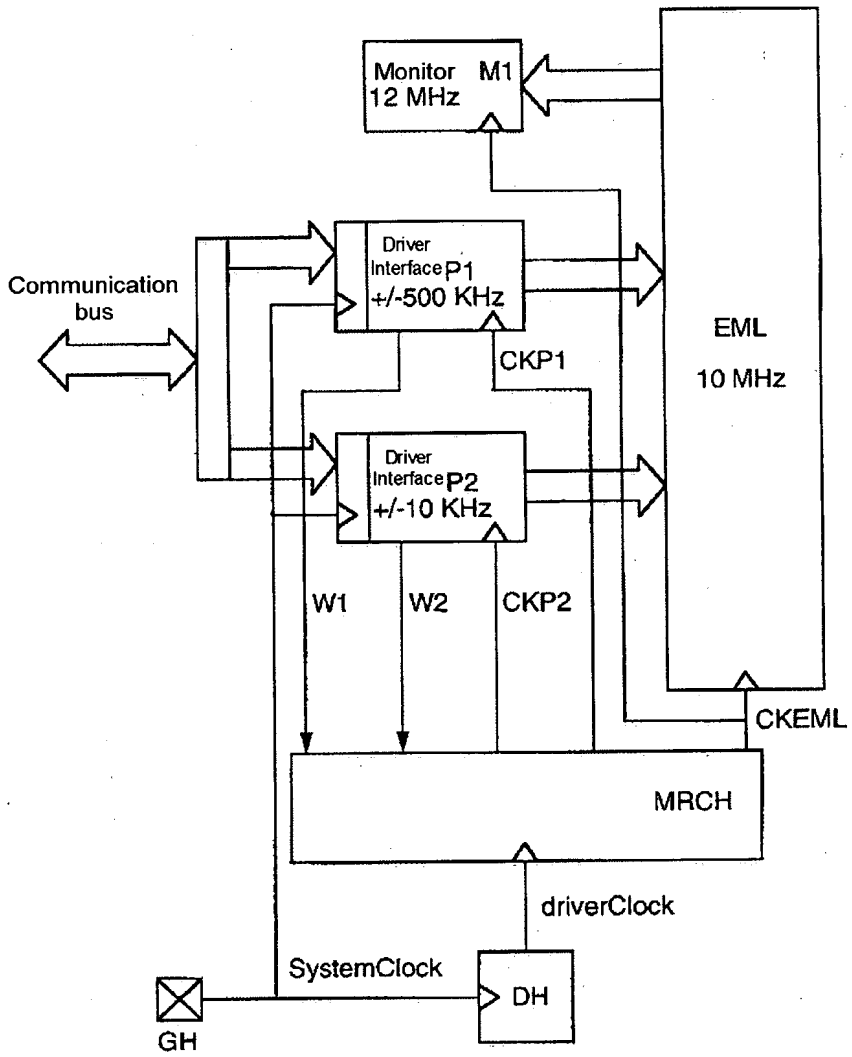
Monitor M1
12 MHz
Communication bus
Driver Interface P1
+/-500 KHz
CKP1
EML
10 MHz
Driver Interface P2
+/-10 KHz
W1
W2
CKP2
CKEML
MRCH
driverClock
SystemClock
DH
GH

FIG.12b

W1	W2	CKP1	CKP2	CKEML
0	0	DriverClock	DriverClock	DriverClock
0	1	Inactive	DriverClock	Inactive
1	0	DriverClock	Inactive	Inactive
1	1	DriverClock	DriverClock	Inactive